IN THE CLAIMS

Claim 1 (currently amended): An image detection processor, comprising:

an image detection processing array including a plurality of image detection processing elements arranged in at least one row; each said image detection processing element of said plurality of image detection processing elements comprising:

a photodetector,

a converter for converting signals from said photodetector into digital signals, and

an adder which receives said digital signals as an input arranged on a plane;

a cumulative adder formed by connecting said adders of a plurality of said image detection processing elements in sequence;

a control circuit which selectively inputs said digital signals of a plurality of said image detection processing elements to said cumulative adder; and

an output port to which processed data outputted from said cumulative adder is supplied in response to image data detected by said photodetector.

Claim 2 (currently amended): An image detection processor, comprising:

an image detection processing array including a plurality of image detection processing elements arranged in a matrix having a plurality of rows; each said image detection processing element of said plurality of image detection processing elements comprising:

a photodetector,

a converter for converting signals from said photodetector into digital signals, and

a first adder which receives said digital signals as an input arranged ~~in a matrix form~~ on a plane;

first cumulative adders formed by connecting said first adders of a plurality of said image detection processing elements in respective rows of said matrix in sequence;

second adders corresponding to respective rows of said image detection processing elements and receiving outputs of final stages of said first cumulative adders of respective rows as inputs;

a second cumulative adder formed by connecting said second adders and cumulatively adding the outputs of said final stages of said first cumulative adders;

a control circuit which selectively inputs said digital signals of a plurality of said image detection processing elements to said cumulative adder; and

an output port to which processed data outputted from said cumulative adder is supplied in response to image data detected by said photodetector.

Claim 3 (currently amended): An image detection processor according to claim 2, wherein said digital signals of said image detection processing elements are all inputted to said first ~~cumulative~~ adders by said control circuit and said processed data outputted from said second ~~cumulative~~ adder is set to the 0-order moment of focused images focused to a group of said image detection processing elements.

Claim 4 (currently amended): An image detection processor according to claim 2, wherein several digital signals selected from said digital signals of said image detection processing elements are inputted to said first ~~cumulative~~ adders by said control circuit and said processed data outputted from said second ~~cumulative~~ adder is set to a partial sum for obtaining an N-order moment of focused images focused to a group of said image detection processing elements, where N is an integer of at least one.

Claim 5 (currently amended): An image detection processor according to claim 2, wherein said converters are operated in accordance with first clocks signals so as to generate said digital signals and said first and second ~~cumulative~~ adders are operated in accordance with second clock signals different from said first clock signals, and said processed data is outputted from said second ~~cumulative~~ adders in order from the lower digit.

Claim 6 (original): An image detection processor according to claim 1, wherein said digital signals outputted from a specific image detection processing element is generated based on an output from said photodetector of said specific image detection processing element and said digital signals from a plurality of image detection processing elements arranged close to said specific image detection processing element.

Claim 7 (original): An image detection processor according to claim 1, wherein all elements are formed into one chip.

Claim 8 (original): An image detection processor according to claim 2, wherein all elements are formed into one chip.

Claims 9 - 14 (canceled)

Please add the following new claims as described below.

Claim 15 (new): An image detection processor, comprising:

an image detection processing element array which includes a plurality of an image detection processing elements arranged in a matrix form, each of the image detection processing elements including a photodetector, a converter for converting signals from said photodetctor into digital signals, and an adder which receives said digital signal and output of a precedent image detection processing element, and outputs an added signal to a next image detection processing element;

a plurality of row lines, each of which is connected to the image detection processing element arranged in a first direction;

a plurality of column lines, each of which is connected to the image detection processing element arranged in a second direction;

a control circuit which selectively inputs digital signals of the image detection processing elements to a corresponding adder by controlling the row and column lines; and

an output port to which processed data outputted from an arbitrary adder is supplied in response to image data detected by said photodetector.

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Claim ~~16~~ (new): An image detection processor comprising:

an image detection processing element array which includes a plurality of image detection processing elements arranged in a matrix form, each of the image detection processing elements including a photodetector, a converter for converting signals from said photodetector into digital signals, and a first adder which receives said digital signal and digital signals of a precedent image detection processing element, and outputs an added signal to a next image detection processing element;

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a plurality of row lines, each of which is connected to the image detection processing element arranged in a first direction;

a plurality of column lines, each of which is connected to the image detection processing element arranged in a second direction;

a control circuit which selectively inputs digital signals of the image detection processing elements to a corresponding first adder by controlling the row and column lines;

second adders corresponding to respective rows of the image detection processing element, and receiving outputs of final stage of the first adders of respective rows and output of precedent second adder; and

an output port to which processed data outputted from a final stage of a second adder is supplied in response to image data detected by said photodetector.

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Claim ~~17~~ (new): An image detection processor comprising:

an image detection processing element array which includes a plurality of image detection processing elements, each of the image detection processing elements including

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a photodetector, a converter for converting signals from said photodetector into digital signals, and an adder which receives said digital signal and output of a precedent image detection processing element, and outputs an added signal to a next image detection processing element;

a plurality of control lines which are connected to the image detection processing elements;

a control circuit which selectively inputs digital signals of the image detection processing elements to a corresponding adder by controlling the row and column lines; and

an output port to which processed data outputted from an arbitrary adder is supplied in response to image data detected by said photodetector.

Claim 12 (new): An image detection processor according to claim 11, wherein said digital signals outputted from a specific image detection processing element is generated based on an output from said photodetector of said specific image detection processing element and said digital signals from a plurality of image detection processing elements arranged close to said specific image detection processing element.

Claim 13 (new): An image detection processor according to claim 11, wherein all elements are formed into one chip.